REMARKS

The amendments to the claims are supported by the original claims. Applicants submit that the amendments do not add any new matter to the disclosure.

Per the note in the first paragraph of the office action, applicants have removed "adapted" from claim 1.

Applicants have provided a replacement abstract which now complies with MPEP 608.01(b).

Regarding the rejections under 35 USC 112, second paragraph, applicants have (a) corrected the lack of antecedent basis with respect to the reference to dynamic time division multiplexing in claim 1, line 3-4, (b) removed the "(...,x,...)" from claim 1, line 8, (c) clarified the reference to n-bit frames, (d) clarified the reference to p bits, and (e) corrected the lack of antecedent basis for the time slot assignment table. Applicants submit that the phrase "the improvement" in claim 1, line 11 is proper Jepson claim language in compliance with 37 CFR 1.75(e). On this basis, applicants submit that the claims are now in compliance with 35 USC 112, second paragraph.

The invention centers on the elimination of the need for a shadow table in a dynamic TDM system which uses a table of time slot assignment data (TSA) to determine which channels are allocated time slots in a bit-frame (transmitted or received). The invention eliminates the need for a shadow table by use of a Nx1 register indicating the status of the channel assignment data contained in the TSA table. The output of the register is provided to a set of p parallel AND gates

which also receive a bit input of the p bits making up an entry in the TSA table where each table entry consists of p bits.

The admitted prior art discloses a dynamic TDM system where a TSA table and a shadow TSA table are used to provide flexibility to the dynamic TDM system. The admitted prior art does not disclose or suggest how to obtain the flexibility of dynamic TDM without use of a shadow TSA table. The admitted prior art does not disclose or suggest the use of a register in combination with a TSA table. The admitted prior art does not disclose or suggest inputting bits from p bit channel identifiers into p parallel AND gates. The admitted prior art does not disclose or suggest the inputting of a register bit value into p parallel AND gates.

Nguyen et al. disclose a method of controlling the transmission of data from a set of modems (handling n-bit words) using a tri-state buffer in combination with a shift register whose output is controlled by channel clock signal operating at 1/n speed of the data clock wherein the shift register output is fed with the modem data to an XOR gate. Nguyen et al. does not disclose or suggest use of resister in combination with a table of time slot assignment data. Nguyen et al. does not disclose or suggest the use of a parallel group of AND gates, nor the feeding of bits of p bit TSA time slot data to p parallel AND gates, nor the feeding of bits from an N x 1 register to the same AND gates. Applicants submit that the combination of the teachings of Nguyen et al. with the admitted prior art would have either resulted modification of the admitted prior art to convert it to a static TDM system or the modification of the interaction of the time slot assigner with the FIFOs containing or receiving data from the respective channels of the system. In either event, applicants submit that that combination would not result in the claimed invention.

For the above reasons, applicants submit that the claims are now patentable over the prior art of record and that the application is now in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,

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